Title: IMAGE-PROCESSING DEVICE, IMAGE-PROCESSING METHOD AND SOLID-STATE IMAGE-PICKUP DEVICE
Inventor: Hiroaki NASU
Atty. Ref.: 9319S-000598

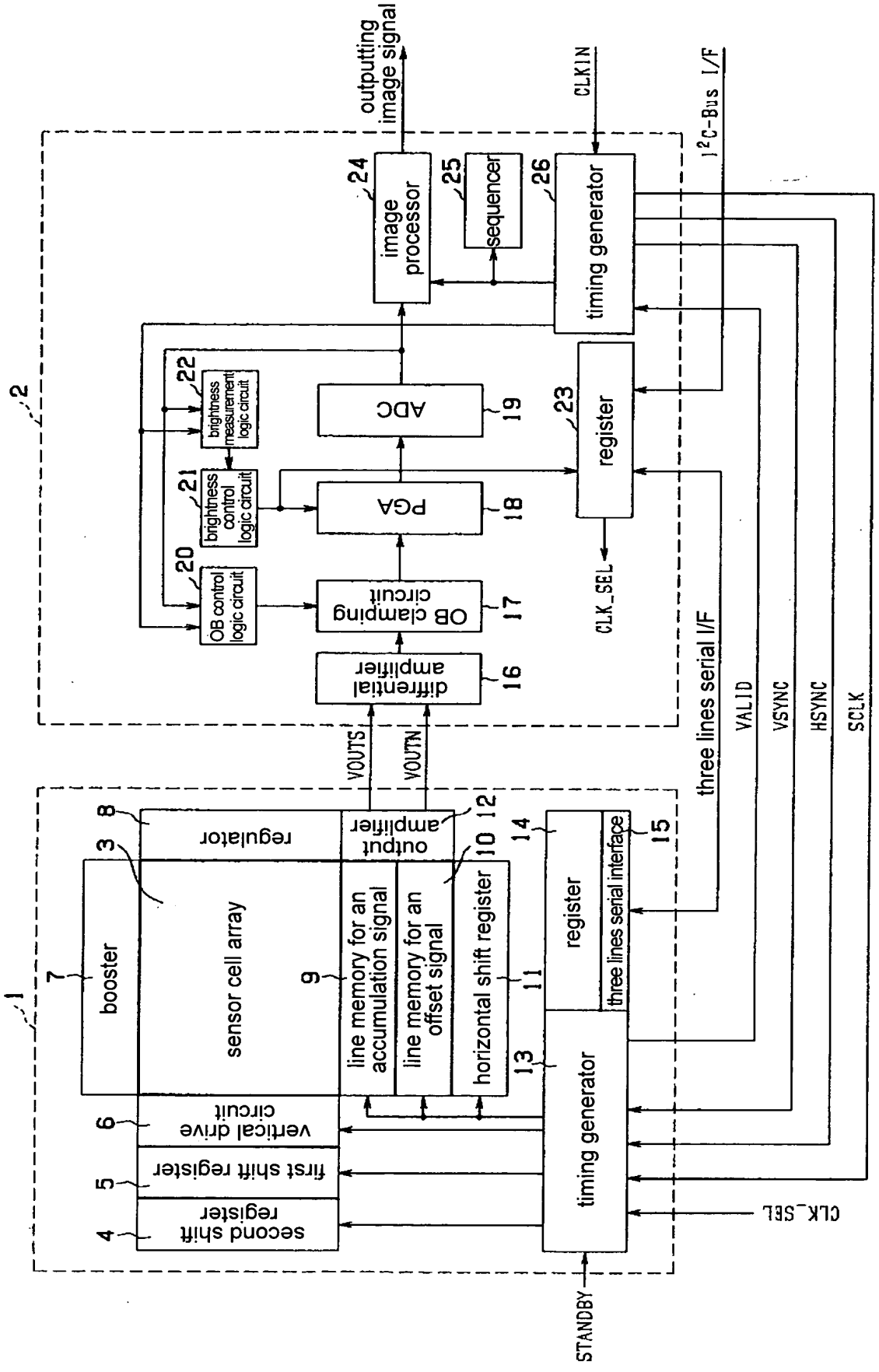

FIG. 1

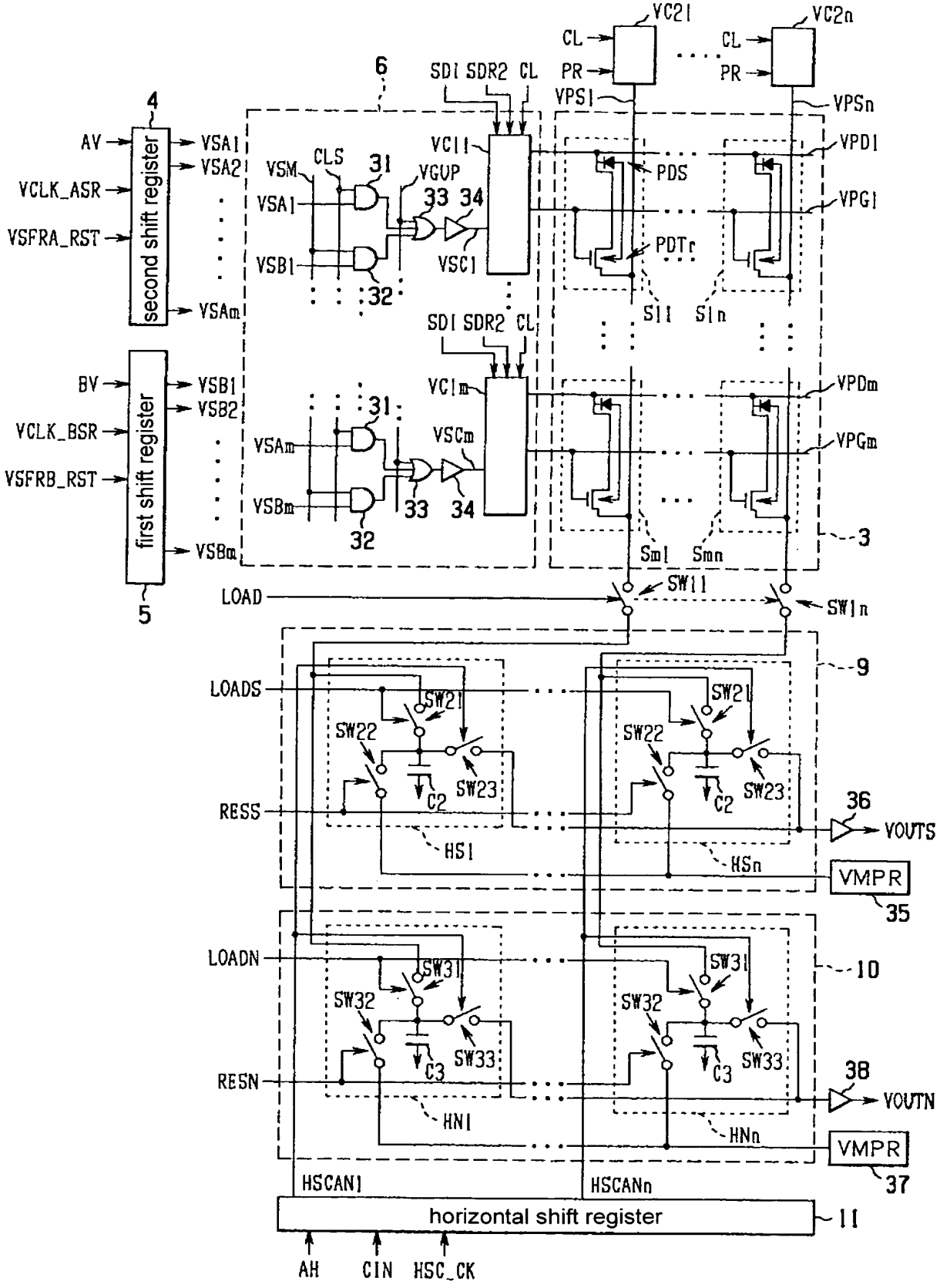
AV
VCLK_ASR
VSFRA_RST
second shift register
VSA1
VSA2
VSAm
4
BV
VCLK_BSR
VSFRB_RST
first shift register
VSB1
VSB2
VSBm
5
6
SDI SDR2 CL
VSM
CLS
31
VSA1
VSB1
VGUP
33 34
VSC1
32
VC11
VC1m
VSCm
VC21
VC2n
CL
PR
VPS1
VPSn
VPD1
VPDm
VPG1
VPGm
PDS
PDTr
S11 S1n
Sm1 Smn
3
LOAD
SW11
SW1n
9
LOADS
SW21
SW22
SW23
C2
RESS
HS1
HSn
36
VOUTS
VMPR
35
10
LOADN
SW31
SW32
SW33
C3
RESN
HN1
HNn
38
VOUTN
37
HSCAN1
HSCANn
horizontal shift register
11
AH
CIN
HSC_CK

FIG. 2

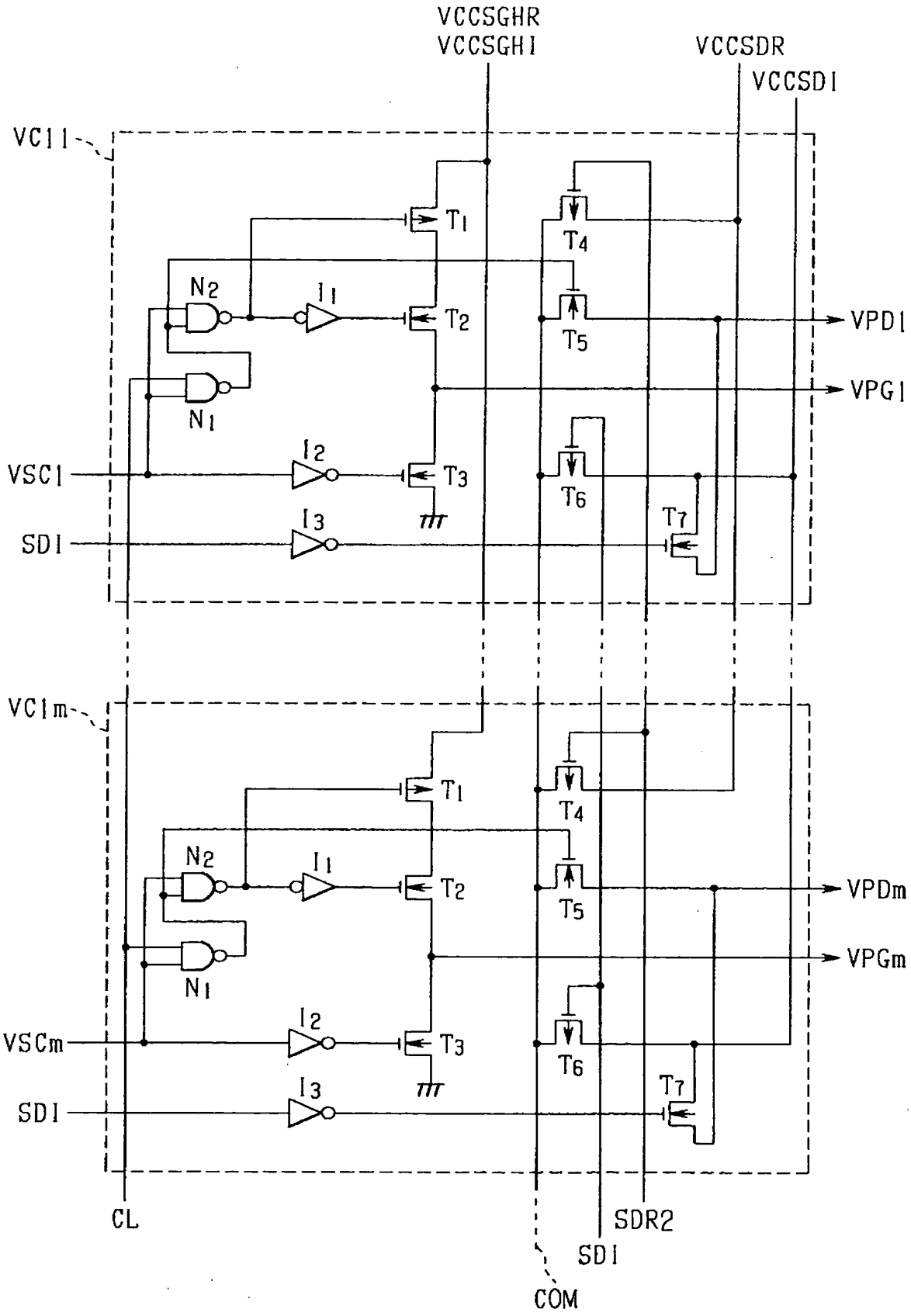
VCCSGHR
VCCSGHI
VCCSDR
VCCSDI
VC1
VC1m
T1
T2
T3
T4
T5
T6
T7
N1
N2
I1
I2
I3
VPD1
VPG1
VPDm
VPGm
VSC1
VSCm
SD1
CL
SDR2
SDI
COM

FIG. 3

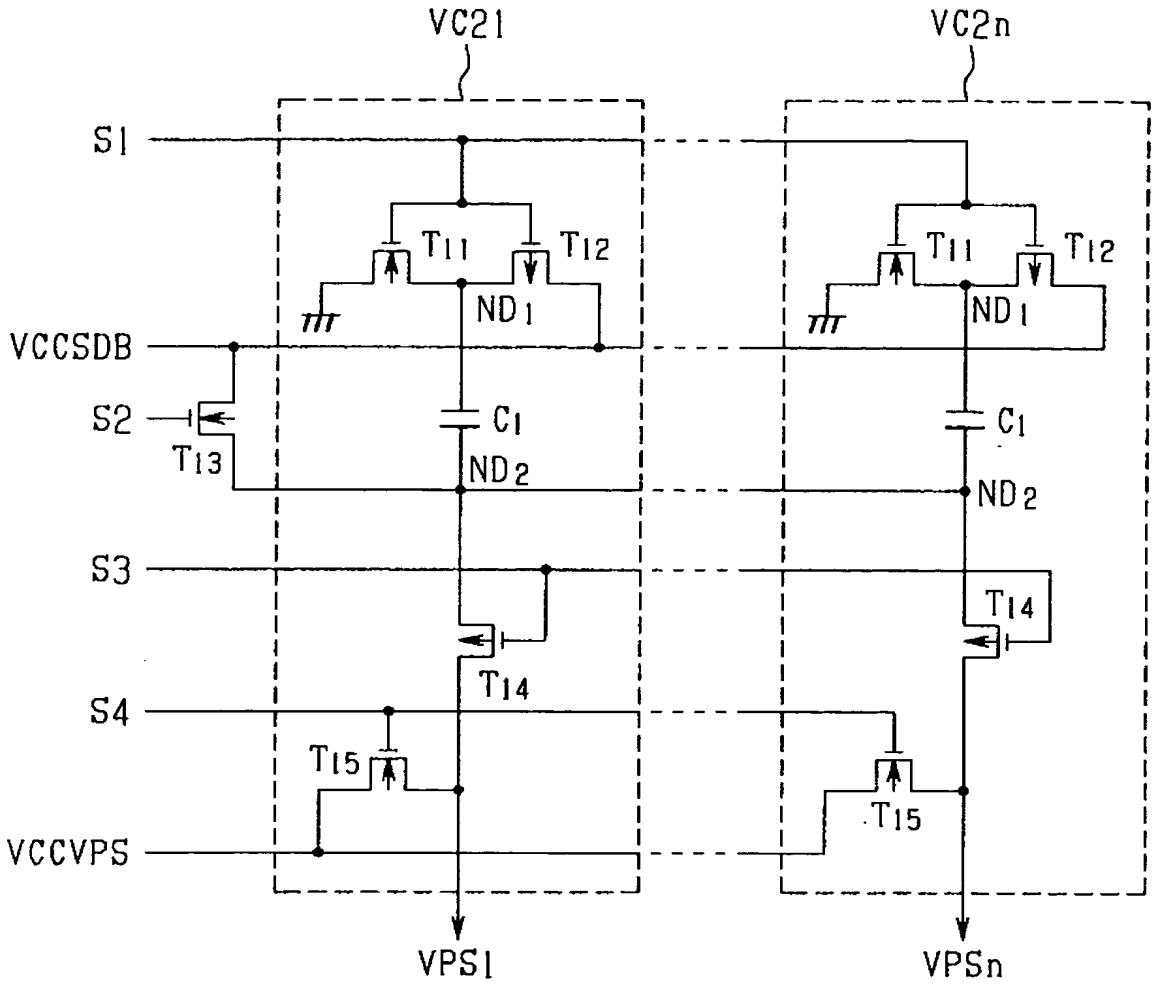
VC21
VC2n
S1
T11
T12
ND1
VCCSDB
S2
T13
C1
ND2
S3
T14
S4
T15
VCCVPS
VPS1
VPSn

FIG. 4A

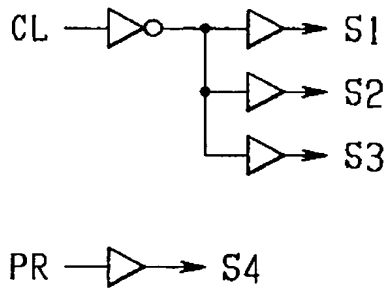
CL
S1
S2
S3
PR
S4

FIG. 4B

States of sensor bias

	state	accumulation	RESS	LOADS	PR	CL	RESN	LOADN
GATE	selected	VCCSGH1	Lo	VCCSGHR	VCCSGHR	VCCSGHR+ VCCSDB X 2	Lo1	VCCSGHR
	non selected		Lo	Lo	Lo	Lo	Lo	Lo
SOURCE	selected	turning "on" (VCCSD1)	VMPR	VCCSGHR-VthS	VCCVPS	VCCSDB X 2	VMPR	VCCSGHR-VthN
DRAIN	selected	VCCSD1	HiZ	VCCSDR	turning "on" (VCCVPS)	turning "on" (VCCSDB X 2)	HiZ	VCCSDR
	non selected		HiZ	VCCSDR	VCCVPS	VCCSDR	HiZ	VCCSDR

FIG. 5

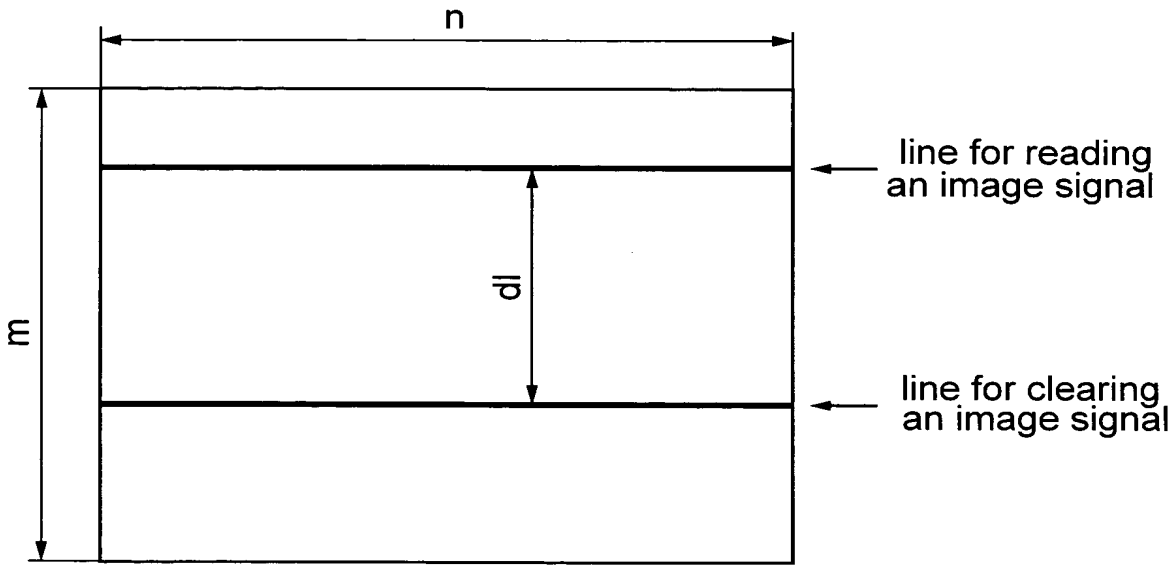
n
m
dl
line for reading an image signal
line for clearing an image signal

FIG. 6

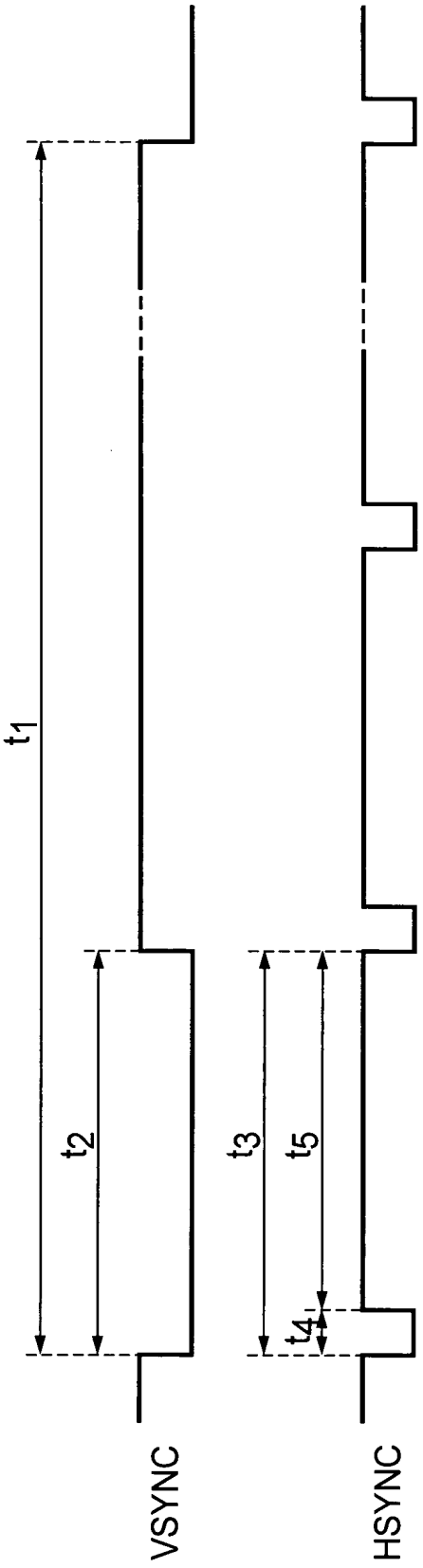

FIG. 7

Title: IMAGE-PROCESSING DEVICE, IMAGE-PROCESSING METHOD AND SOLID-STATE IMAGE-PICKUP DEVICE
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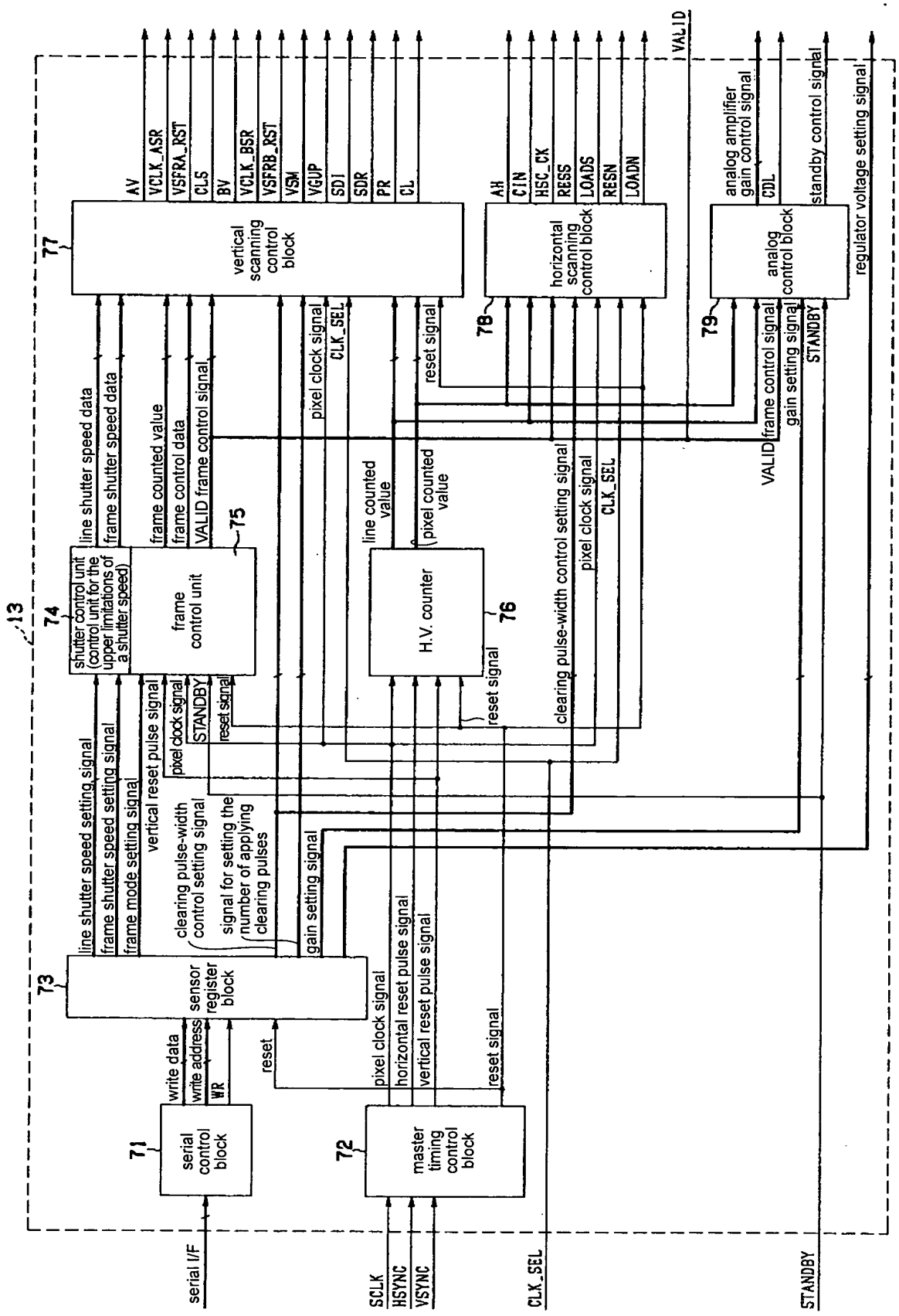

FIG. 8

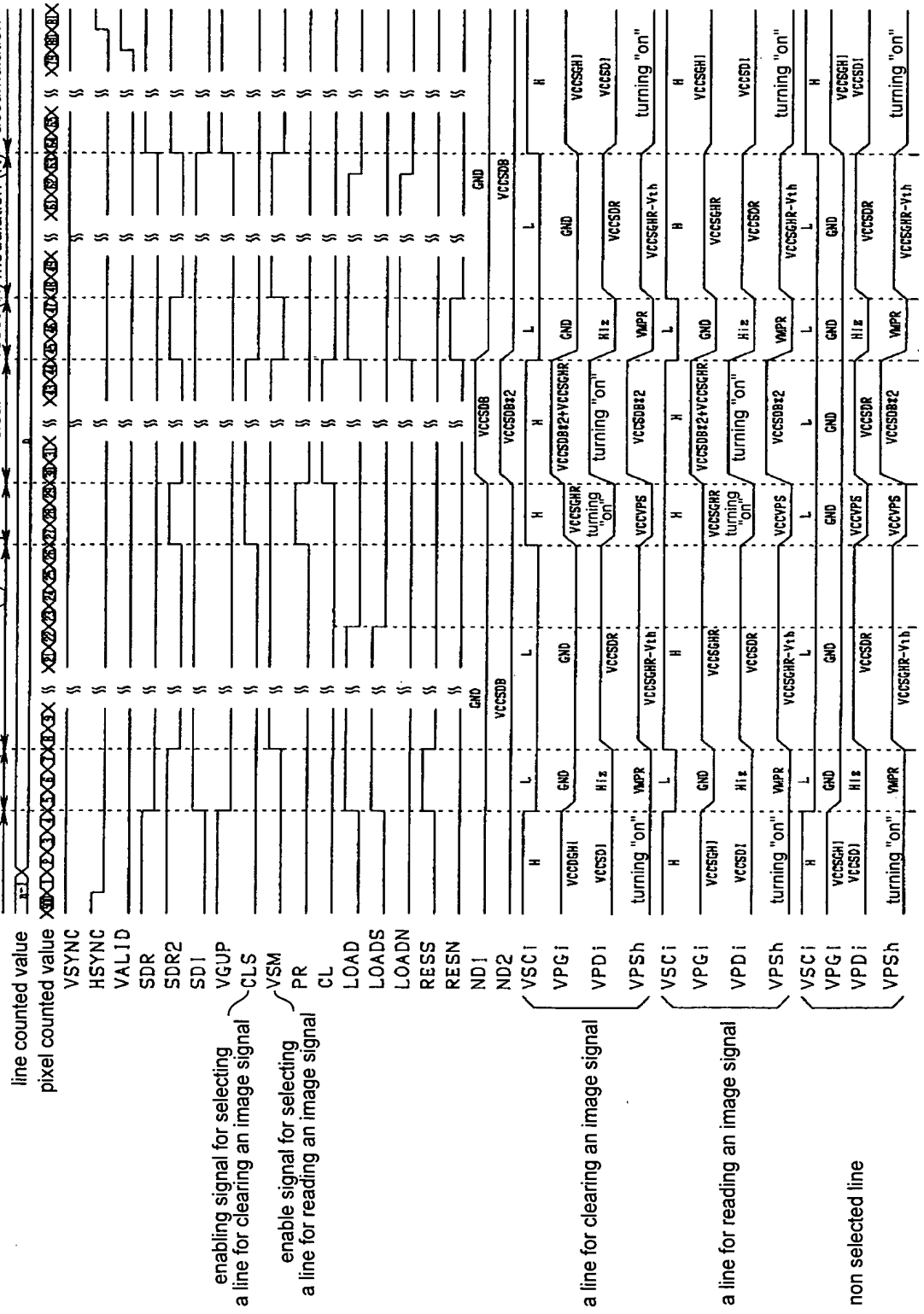
accumulation
reset(S)
modulation (S)
preset.
clear
reset (N)
modulation (N)
accumulation
line counted value
pixel counted value
VSYNC
HSYNC
VALID
SDR
SDR2
SDI
VGUP
CLS
VSM
PR
CL
LOAD
LOADS
LOADN
RESS
RESN
ND1
ND2
VSCi
VPGi
VPDi
VPSh
enabling signal for selecting a line for clearing an image signal
enable signal for selecting a line for reading an image signal
a line for clearing an image signal
a line for reading an image signal
non selected line
H
L
GND
VCCSDB
VCCSDB×2
VCCSDB×2+VCCSHR
VCCSHR
VCCSDR
VCCPS
VMPR
VCCSHR-Vth
turning "on"
Hiz

FIG. 9

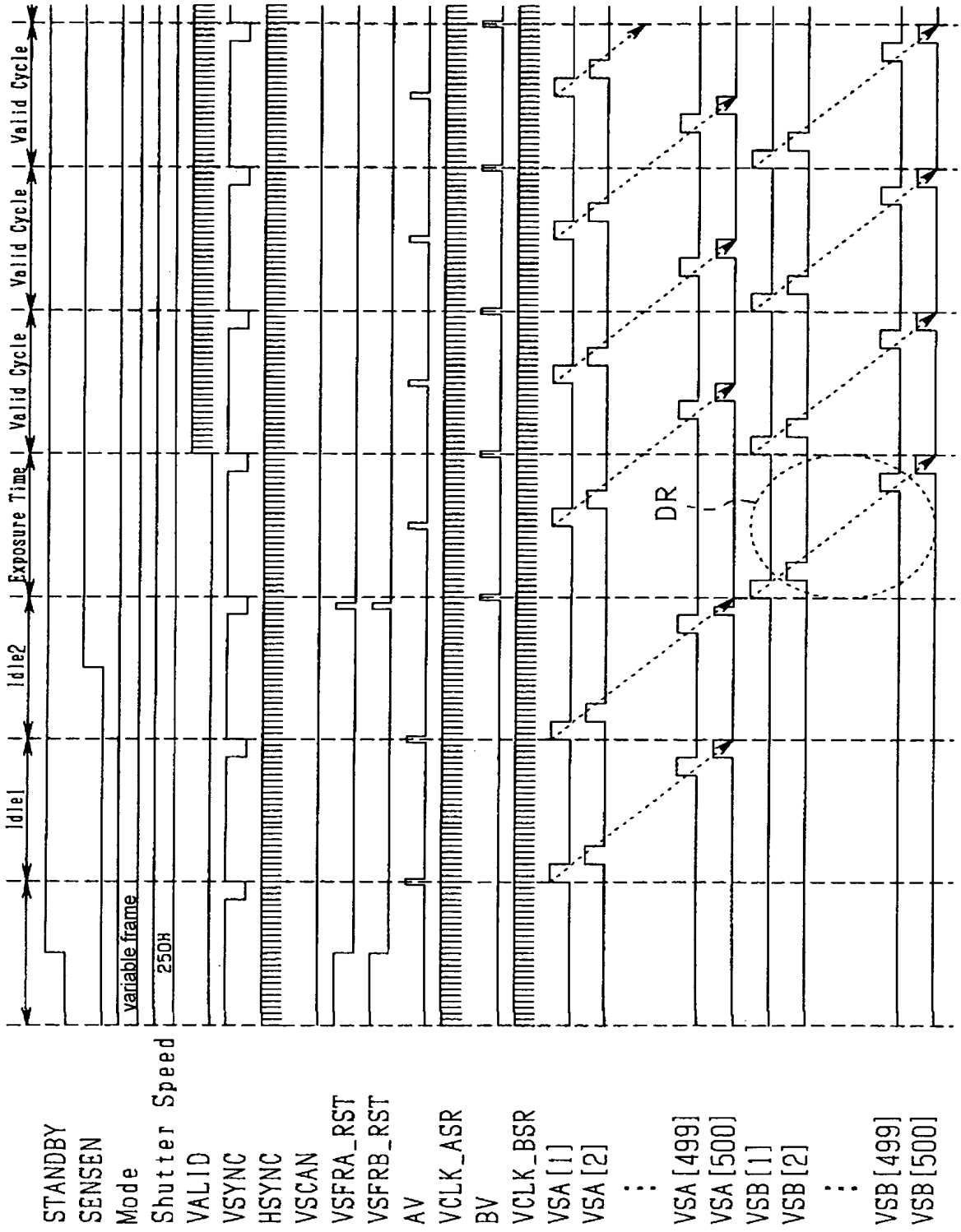
Idle1
Idle2
Exposure Time
Valid Cycle
Valid Cycle
Valid Cycle
Valid Cycle
Valid Cycle
variable frame
250H
STANDBY
SENSEN
Mode
Shutter Speed
VALID
VSYNC
HSYNC
VSCAN
VSFRA_RST
VSFRB_RST
AV
VCLK_ASR
BV
VCLK_BSR
VSA[1]
VSA[2]
VSA[499]
VSA[500]
VSB[1]
VSB[2]
VSB[499]
VSB[500]
DR

FIG. 10

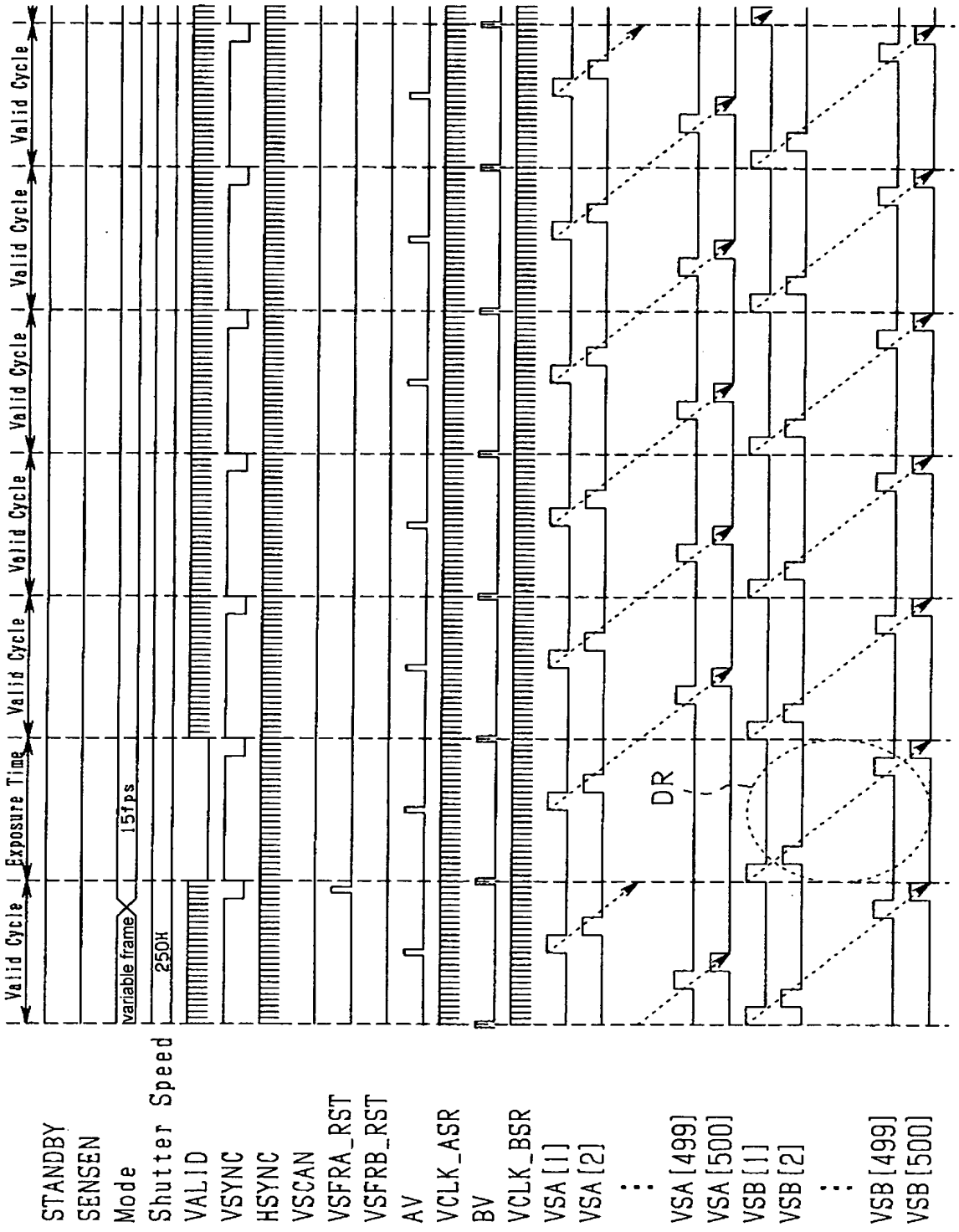
Valid Cycle
Exposure Time
Valid Cycle
Valid Cycle
Valid Cycle
Valid Cycle
Valid Cycle
Valid Cycle
variable frame
15fps
250H
STANDBY
SENSEN
Mode
Shutter Speed
VALID
VSYNC
HSYNC
VSCAN
VSFRA_RST
VSFRB_RST
AV
VCLK_ASR
BV
VCLK_BSR
VSA[1]
VSA[2]
VSA[499]
VSA[500]
VSB[1]
VSB[2]
VSB[499]
VSB[500]
DR

FIG. 11

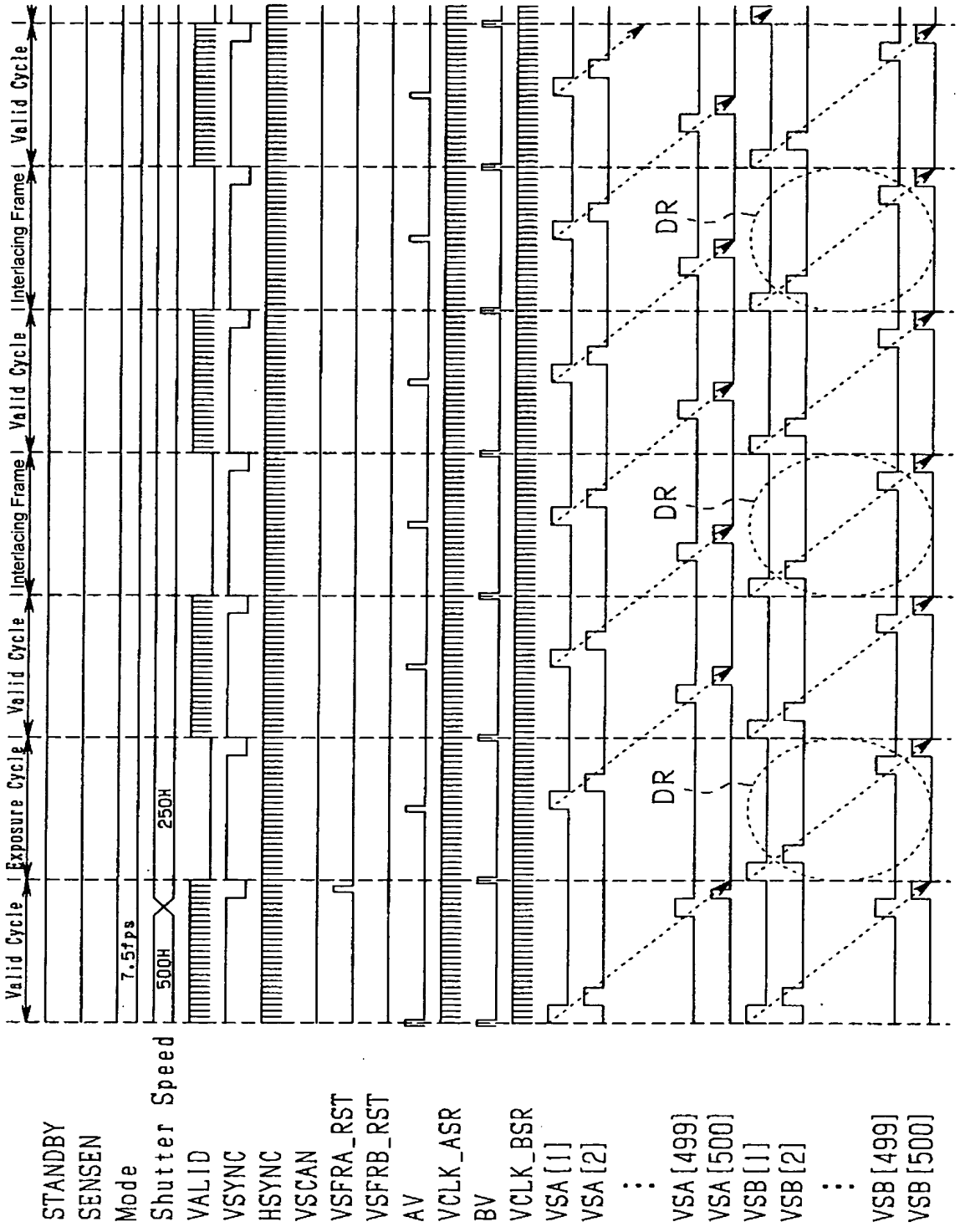
Valid Cycle
Exposure Cycle
Valid Cycle
Interlacing Frame
Valid Cycle
Valid Cycle
Interlacing Frame
Valid Cycle
7.5fps
500H
250H
STANDBY
SENSEN
Mode
Shutter Speed
VALID
VSYNC
HSYNC
VSCAN
VSFRA_RST
VSFRB_RST
AV
VCLK_ASR
BV
VCLK_BSR
VSA[1]
VSA[2]
VSA[499]
VSA[500]
VSB[1]
VSB[2]
VSB[499]
VSB[500]
DR
DR
DR

FIG. 12

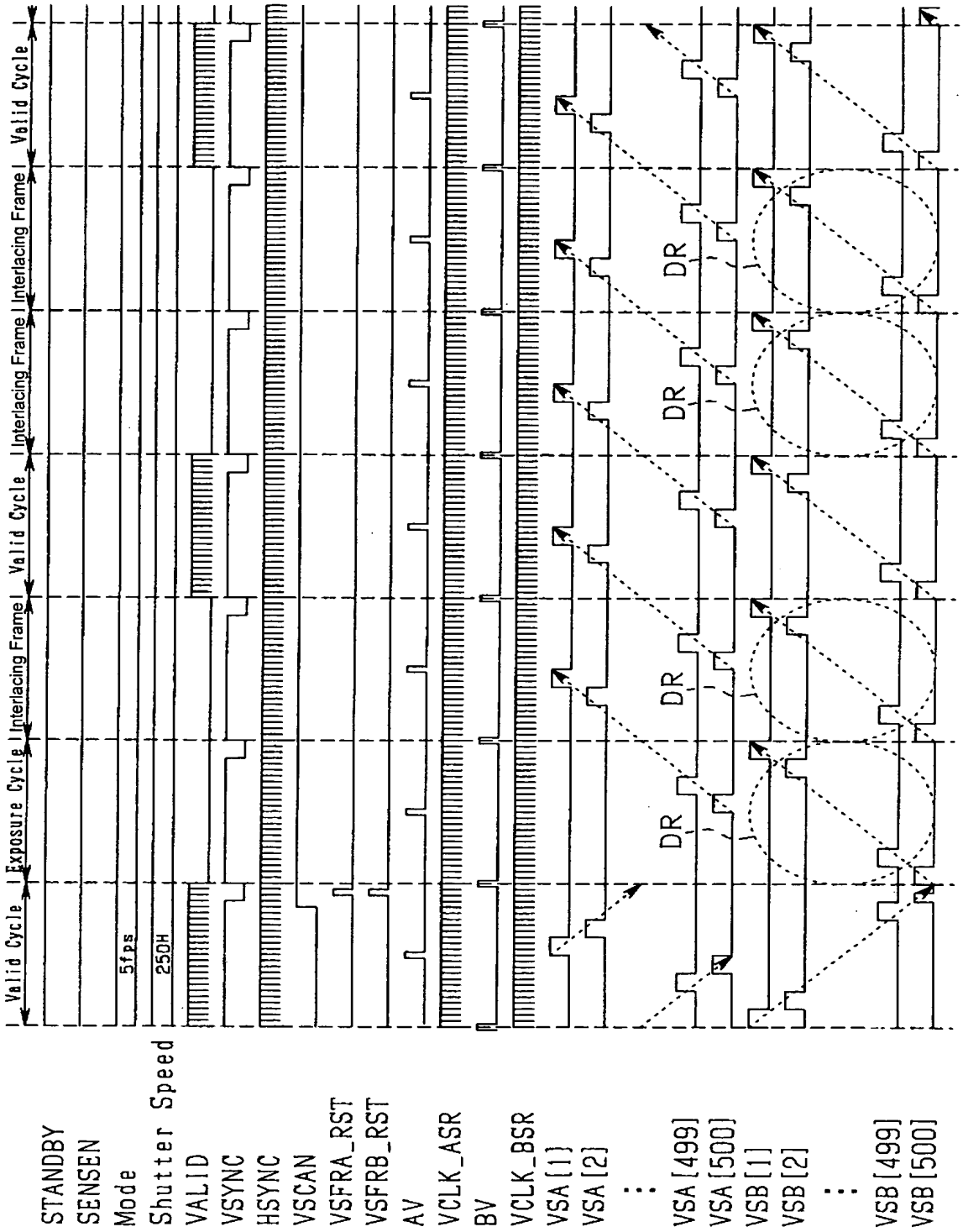
Valid Cycle
Exposure Cycle
Interlacing Frame
Valid Cycle
Interlacing Frame
Interlacing Frame
Valid Cycle
STANDBY
SENSEN
Mode
Shutter Speed
VALID
VSYNC
HSYNC
VSCAN
VSFRA_RST
VSFRB_RST
AV
VCLK_ASR
BV
VCLK_BSR
VSA[1]
VSA[2]
VSA[499]
VSA[500]
VSB[1]
VSB[2]
VSB[499]
VSB[500]
5fps
250H
DR
DR
DR
DR

FIG. 13

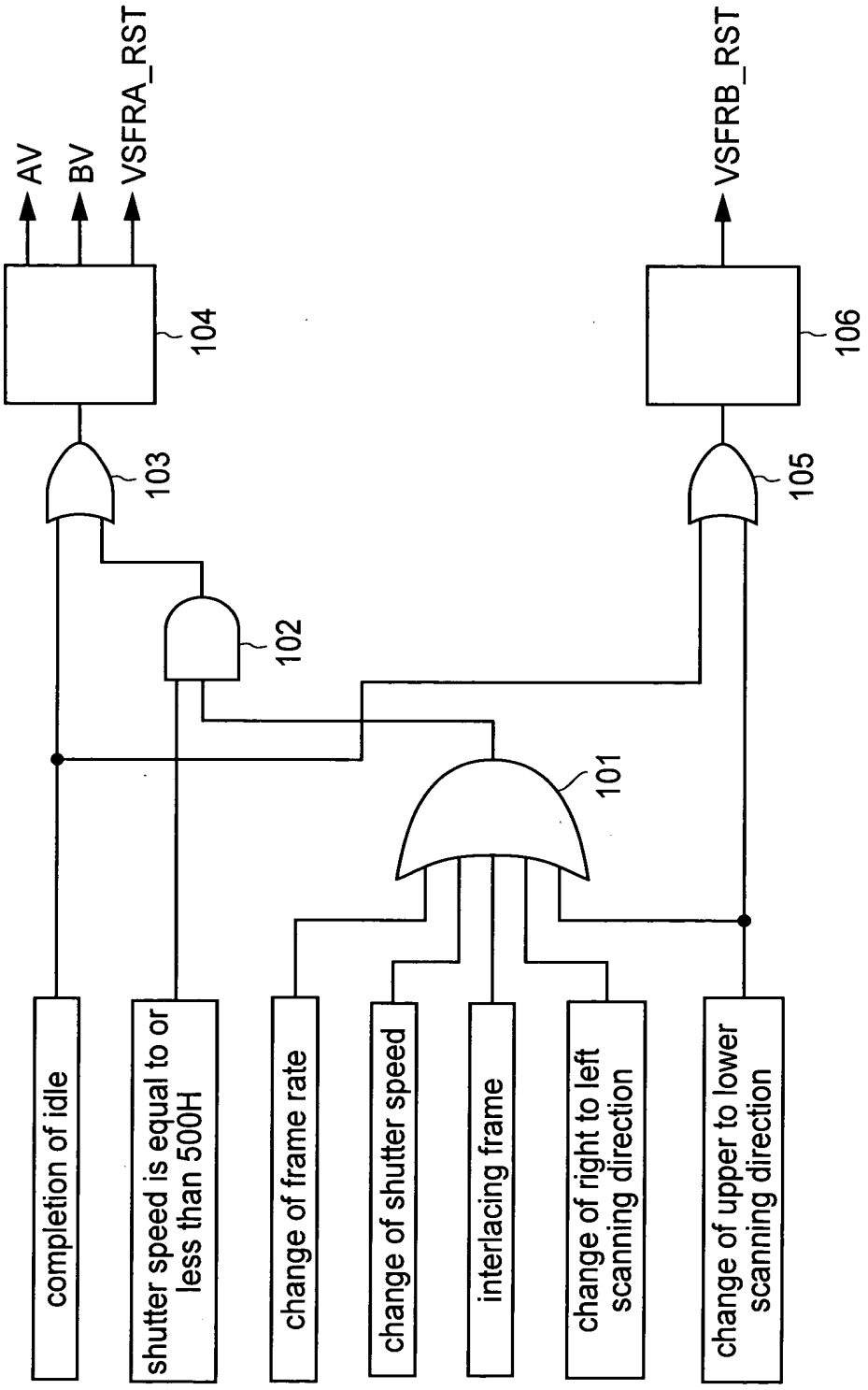
AV
BV
VSFRA_RST
VSFRB_RST
104
106
103
105
102
101
completion of idle
shutter speed is equal to or less than 500H
change of frame rate
change of shutter speed
interlacing frame
change of right to left scanning direction
change of upper to lower scanning direction

FIG. 14